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HfON/LaON as Charge-Trapping Layer for Nonvolatile Memory Applications

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Abstract— **The charge-trapping characteristics of HfON/LaON composite film (denoted as HfLaON) were investigated based on an Al/Al_2O_3/HfLaON/SiO_2/Si (MONOS) capacitor. The physical properties of the high-*k* film were analyzed by transmission electron microscopy and electron diffraction spectroscopy. Compared with another MONOS capacitor with nitrided La_2O_3 as charge-trapping layer, the one with HfLaON showed better memory characteristics in terms of larger memory window, higher program speed (6.3 V at +14 V for 100 μs), and smaller charge loss (8.2% after 10^4 sec), due to the HfLaON composite film exhibiting an amorphous structure and the suppressed formation of an interlayer at the HfLaON/SiO_2 interface.**

Keywords-nonvolatile memory; charge-trapping; HfLaON.

I. INTRODUCTION

Charge-trapping flash memories with Metal-Oxide-Nitride-Oxide-Si (MONOS) structure have attracted increasing attention as a promising candidate for next-generation nonvolatile memories, mainly due to their lower power consumption, higher reliability, and stronger scaling ability than their floating-gate counterparts [1]-[5]. Si_3N_4 was the first dielectric used as the charge-trapping layer (CTL). Then, many efforts have been spent to study high-*k* dielectrics as CTL for continually scaling the cell size and improving the charge-storage capacity [1]-[5]. Among various high-*k* dielectrics, La_2O_3 is a promising candidate as CTL, mainly because of its high dielectric constant, proper conduction-band offset with Si, and deep traps [2], [6]. Moreover, previous work has demonstrated that the charge-trapping characteristics of La_2O_3 can be further improved by nitrogen incorporation in terms of higher program/erase (P/E) speeds and better data retention [5]. However, La_2O_3 is easy to react with the SiO_2 tunneling oxide, resulting in a La-silicate interlayer at the La_2O_3/SiO_2 interface after post-deposition annealing [5], [7]. The formation of this interlayer consumes the SiO_2, and the traps associated with the interlayer can also act as a medium to accelerate stored electrons escaping through the CTL into the Si substrate [4]. Therefore, it is harmful to the data retention of the memory device. On the other hand, HfON, which shows a smaller dielectric constant (~ 22) than La_2O_3 (~ 30) [3], [6], is well-known for its thermodynamic stability with SiO_2; consequently, a good interface can be expected between HfON and SiO_2 [6]. Both La_2O_3 and HfON films present poor thermal stability with a low crystallization temperature; on the contrary, it is widely reported that the HfLaON composite film displays better thermal stability with a higher crystallization temperature than the HfON or La_2O_3 film [8]. Therefore, based on MONOS capacitors, this work aims to study the charge-trapping characteristics of HfLaON by comparing with nitrided La_2O_3.

II. EXPERIMENTS

MONOS capacitors were fabricated on p-type (100) substrate. After a standard RCA cleaning, 2-nm SiO_2 tunneling layer (TL) was grown on the wafer by thermal dry oxidation. Then, 2-nm HfON was deposited as the CTL on the SiO_2 by reactive sputtering using a Hf target in a mixed Ar and N_2 ambient. Following that, 2-nm La_2O_3 was deposited *in situ* also as the CTL using a La_2O_3 target in an Ar/N_2 ambient. Then, 15-nm Al_2O_3 as blocking layer (BL) was deposited by means of atomic layer deposition using trimethyl-aluminum ($Al(CH_3)_3$) and H_2O as precursors at 300 ^oC. Then, the samples went through a post-deposition annealing (PDA) in N_2 ambient at 850 ^oC for 30 s. In the next step, Al was evaporated and patterned as gate electrode with a diameter of 100 μm. Finally, Al was also evaporated at the wafer backside to form ohmic contact, followed by forming-gas annealing at 300 ^oC for 20 min. For comparison, a control device with 4-nm nitrided La_2O_3 layer as CTL was also fabricated using the same process as mentioned above. The MONOS devices with and without Hf incorporation are denoted as HfLaON and LaON respectively. The physical characteristics of the high-*k* dielectric films were obtained by transmission electron microscopy (TEM) and electron diffraction spectroscopy (EDS). The electrical characteristics of the memory capacitors were measured by HP4284A LCR meter and HP4156A semiconductor parameter analyzer. The Fowler-Nordheim method by applying a gate voltage (V_G) between the gate electrode and the substrate was used to program/erase the memory devices.

III. RESULTS AND DISSCUSION

The inset of Fig. 1 shows the cross-sectional TEM image of the HfLaON sample, from which the thickness of each layer (SiO_2/HfLaON/Al_2O_3) is determined to be 2.0 nm/3.8 nm/14.6 nm respectively. Moreover, an abrupt interface between the HfLaON and SiO_2 tunneling oxide is also

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observed, indicating negligible formation of an interlayer at the HfLaON/SiO_2 interface. The compositional depth profile of the HfLaON sample is also shown in Fig. 1, where the Hf element is located closer to the Si substrate than the La element. This observation is in accordance with the deposition sequence, and contributes to a good HfLaON/SiO_2 interface, because Hf is chemically more stable than La when contacting with SiO_2 [5]-[7]. The atomic ratio of La/(La+Hf) in the HfLaON composite film is calculated to be 46 % from the EDS analysis, and this high La content is helpful to keep the HfLaON film amorphous even at a high annealing temperature up to 1000 °C [8].

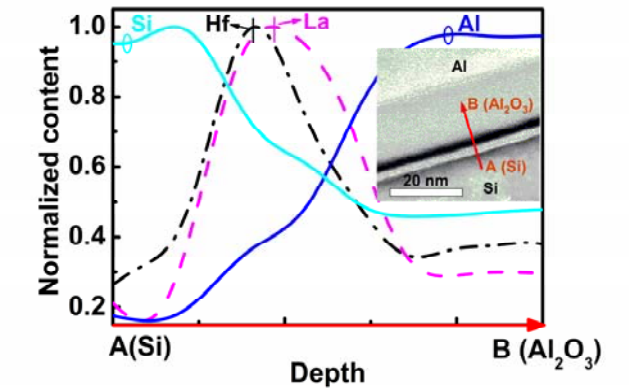


Fig. 1. Compositional depth profile of the HfLaON sample along the designated route in the inner TEM image (A→B). The inset shows the cross-sectional TEM image of the HfLaON sample.

Fig. 2 shows the P/E transient characteristics of the HfLaON and LaON samples, where the HfLaON sample displays higher P/E speeds and larger memory window than the LaON one under the same operating conditions. As V_G is increased from +10 V to +14 V with a pulse width of 100 μs, the V_{FB} shift (ΔV_{FB}) increases from 3.0 V to 4.4 V for the LaON sample. For comparison, the HfLaON sample shows a ΔV_{FB} increasing from 3.2 V to 6.3 V under the same conditions, demonstrating its higher program speed, which is especially obvious under higher operating voltages. The higher P/E speeds should be due to the higher charge-trapping efficiency of the HfLaON sample with an amorphous HfLaON composite film as the CTL. For the LaON sample, its LaON film shows poly-crystalline structure [5], where the grain boundaries can provide a leakage path to facilitate electrons escaping from the CTL to the gate electrode rather than being trapped in the charge-trapping film, thus leading to a lower trapping efficiency [1], [5]. In addition, due to the shortened tunneling path, the electrons stored in the traps associated with the non-stoichiometric interlayer at the CTL/SiO_2 interface are also easier to escape from the CTL into the Si substrate than those located in the bulk traps [4]. The above phenomena are more severe under higher electric field (E_{ox}), corresponding to higher V_G applied on the memory device, because the tunneling probability increases rapidly with the E_{ox}. This should be the reason that the HfLaON sample exhibits a much higher program speed than the LaON one at higher gate voltage (6.3 V versus 4.4 V at +14 V for 100 μs) compared with that operated at lower gate voltage (3.2 V versus 2.9 V at +10 V for 100 μs).

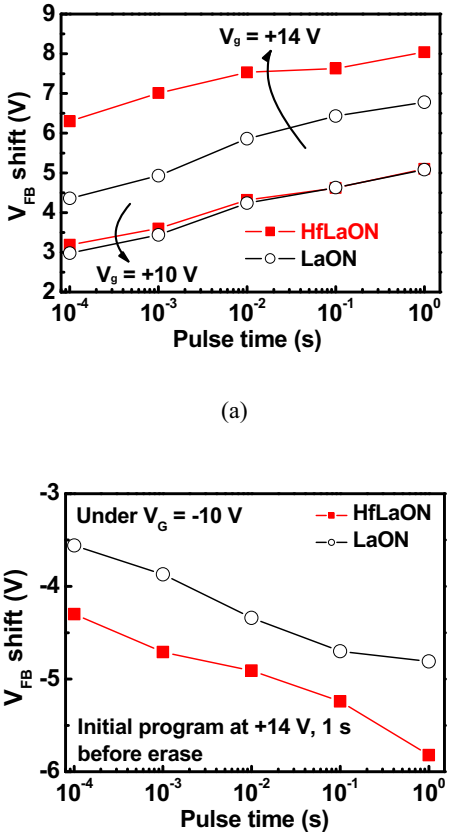
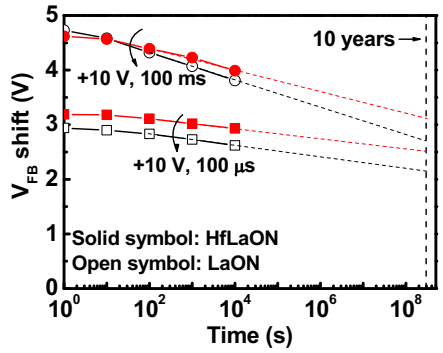


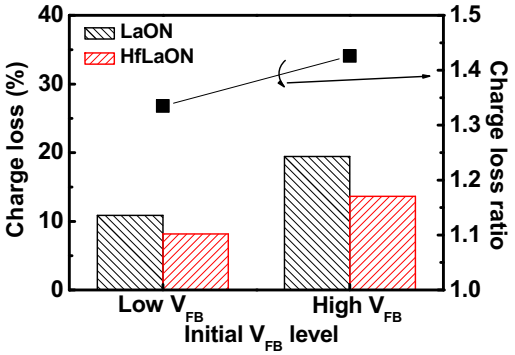
Fig. 2. (a) Program and (b) erase transient characteristics of the MONOS capacitors with and without Hf incorporation.

Fig. 3(a) shows the retention characteristics of the HfLaON and LaON samples measured at room temperature. For fair compassion, both samples are programmed to obtain a similar initial ΔV_{FB}. With an initial ΔV_{FB} of about ~ 3.1 V, the decay rate of the data retention is 65 mV/dec and 80 mV/dec for the HfLaON and LaON samples respectively. The worse data retention of the LaON sample should be ascribed to the poly-crystalline structure of the LaON film, where the electrons trapped along the grain boundaries are easier to escape, thus deteriorating the data retention [1], [5]. Moreover, the formation of La silicate interlayer at the CTL/SiO_2 interface could also contribute to its poor retention property, because the traps associated with the interlayer can accelerate the charge loss [4]. It is also observed in Fig. 3(b) that the charge loss (Q_{loss}) is dependent on the initial V_{FB} level, where the charge loss of the higher-V_{FB} state is more severe than that of the lower-V_{FB} state. It is reported that the injected electrons tend to fill firstly the deep traps and then the shallow ones under the program mode [9]. The electrons in the shallow traps are easier to escape than those in the deep traps during the retention mode, thus leading to more severe charge loss for the higher-V_{FB} state. This is the situation for both HfLaON and LaON samples here.

Furthermore, the charge-loss ratio, which is defined as the ratio of Q_{loss} after 10^4 s between the LaON and HfLaON samples, is higher for the higher-V_{FB} state than for the lower-V_{FB} state, indicating more shallow traps in the LaON sample.



(a)



(b)

Fig. 3. (a) Retention characteristics of the HfLaON and LaON samples with different initial V_{FB} levels measured at room temperature. (b) Charge loss rate after 10^4 s under different initial V_{FB} levels for the HfLaON and LaON samples.

IV. Conclusions

In summary, the charge-trapping characteristics of HfLaON composite film are investigated based on MONOS-type capacitor. The memory device with HfLaON as the charge-trapping layer shows larger memory window, higher P/E speeds and better data retention than the one with nitrided La_2O_3 as the charge-trapping layer. Therefore, the HfLaON film is a promising charge-trapping layer for high-performance nonvolatile memory applications.

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